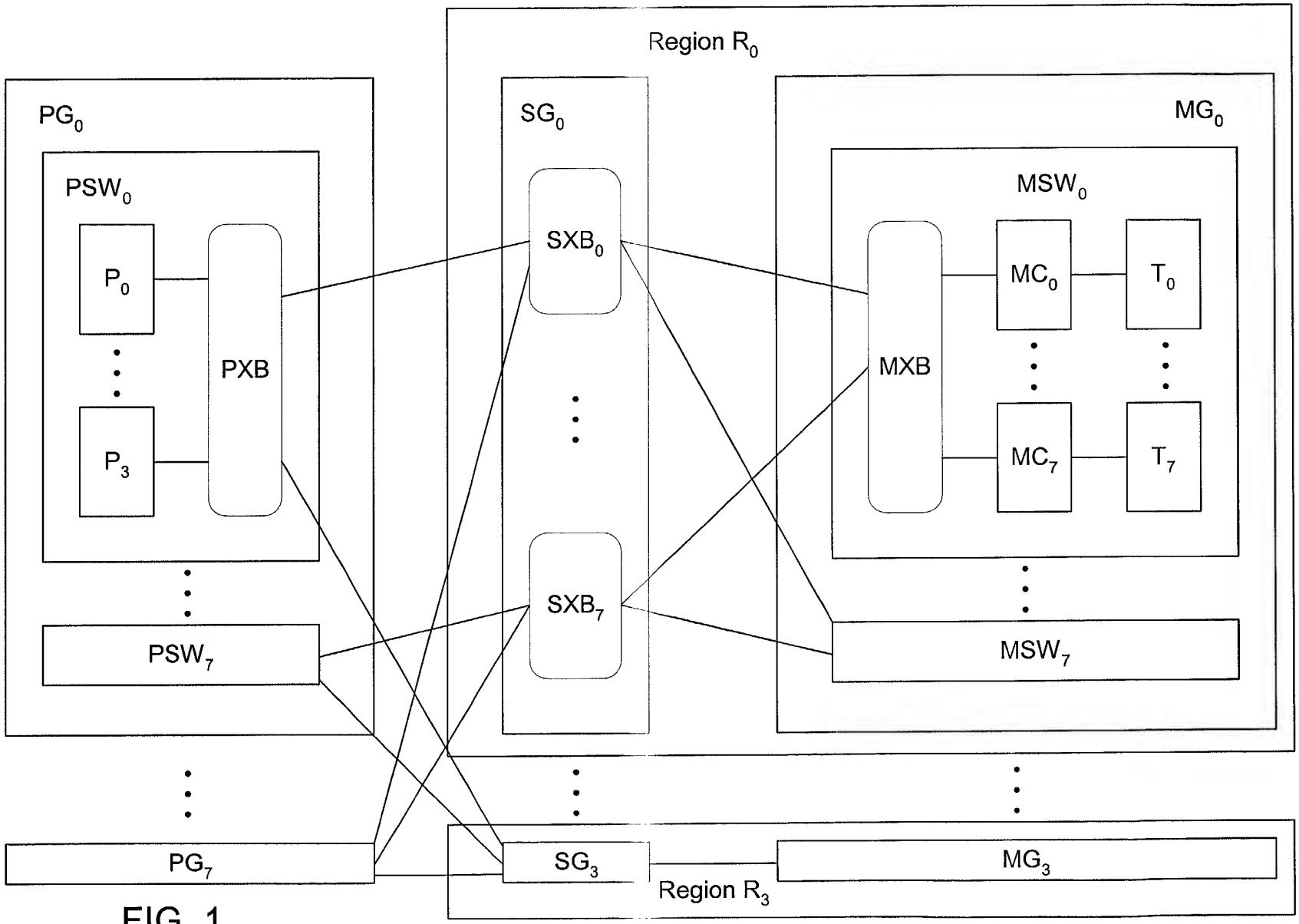


FIG. 1

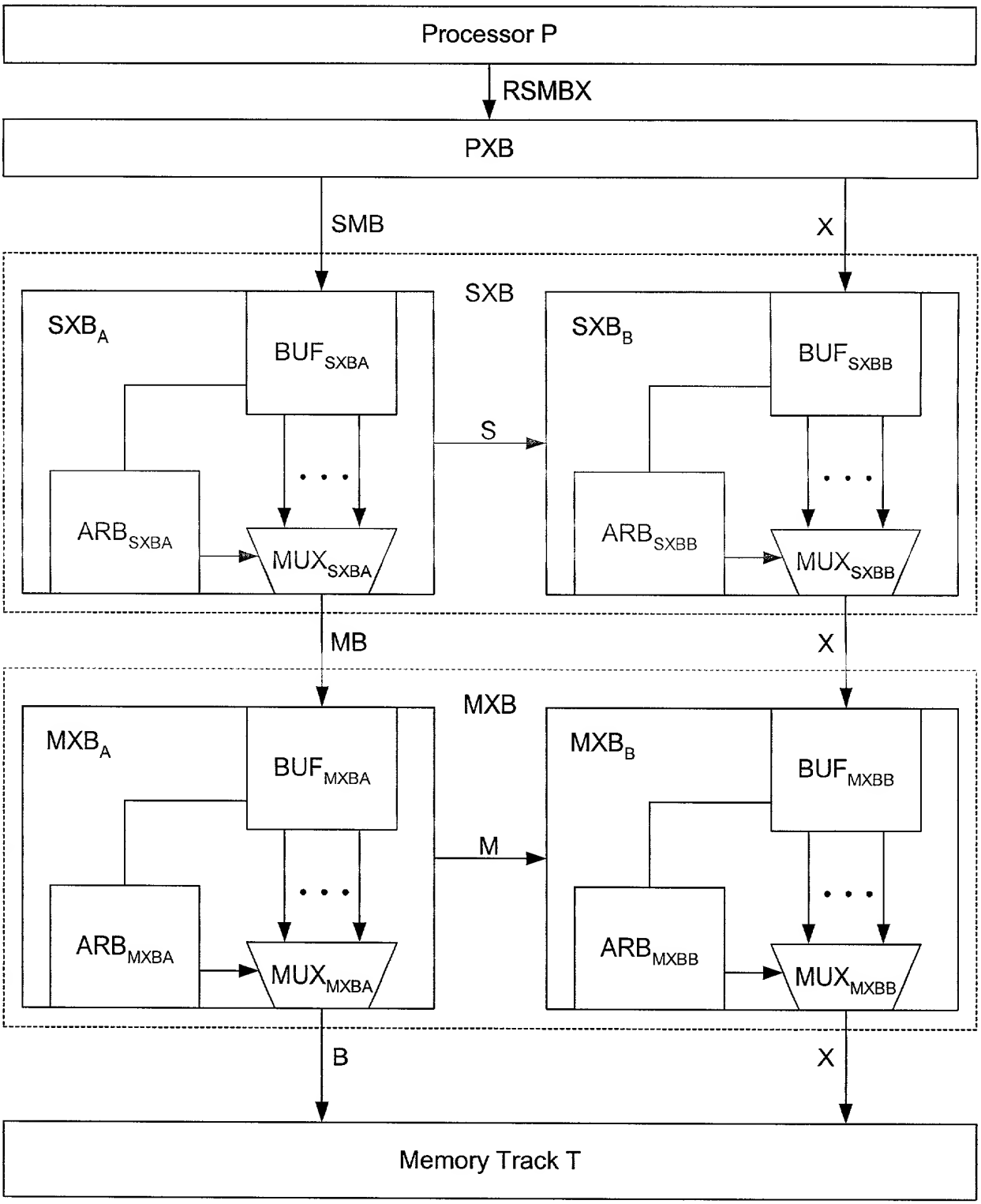

Processor P
RSMBX
PXB
SMB
X
SXB
SXB_A
BUF_SXBA
SXB_B
BUF_SXBB
S
ARB_SXBA
MUX_SXBA
ARB_SXBB
MUX_SXBB
MB
X
MXB
MXB_A
BUF_MXBA
MXB_B
BUF_MXBB
M
ARB_MXBA
MUX_MXBA
ARB_MXBB
MUX_MXBB
B
X
Memory Track T

FIG. 2

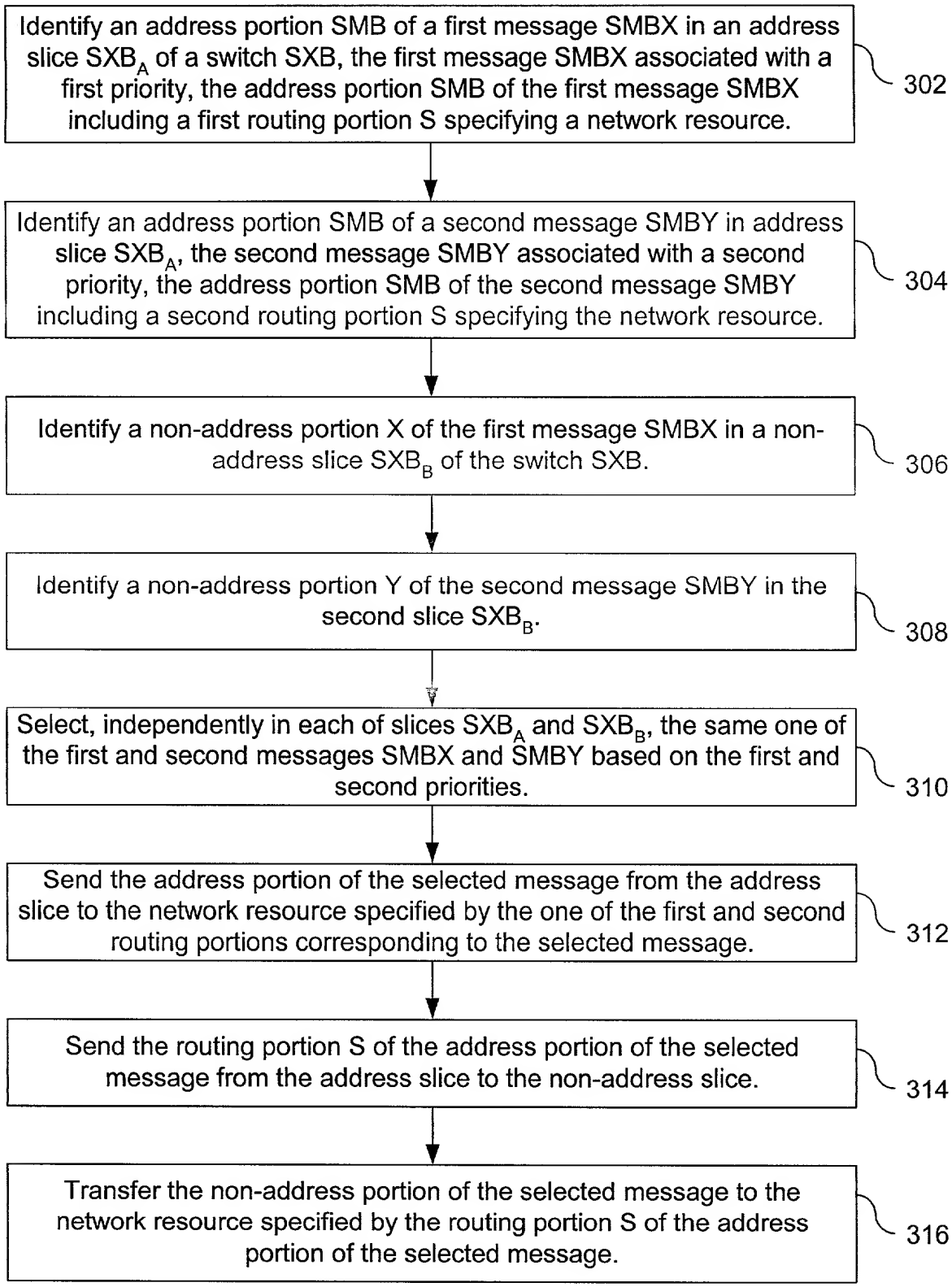

Identify an address portion SMB of a first message SMBX in an address slice SXB_A of a switch SXB, the first message SMBX associated with a first priority, the address portion SMB of the first message SMBX including a first routing portion S specifying a network resource.
302
Identify an address portion SMB of a second message SMBY in address slice SXB_A, the second message SMBY associated with a second priority, the address portion SMB of the second message SMBY including a second routing portion S specifying the network resource.
304
Identify a non-address portion X of the first message SMBX in a non-address slice SXB_B of the switch SXB.
306
Identify a non-address portion Y of the second message SMBY in the second slice SXB_B.
308
Select, independently in each of slices SXB_A and SXB_B, the same one of the first and second messages SMBX and SMBY based on the first and second priorities.
310
Send the address portion of the selected message from the address slice to the network resource specified by the one of the first and second routing portions corresponding to the selected message.
312
Send the routing portion S of the address portion of the selected message from the address slice to the non-address slice.
314
Transfer the non-address portion of the selected message to the network resource specified by the routing portion S of the address portion of the selected message.
316

FIG. 3

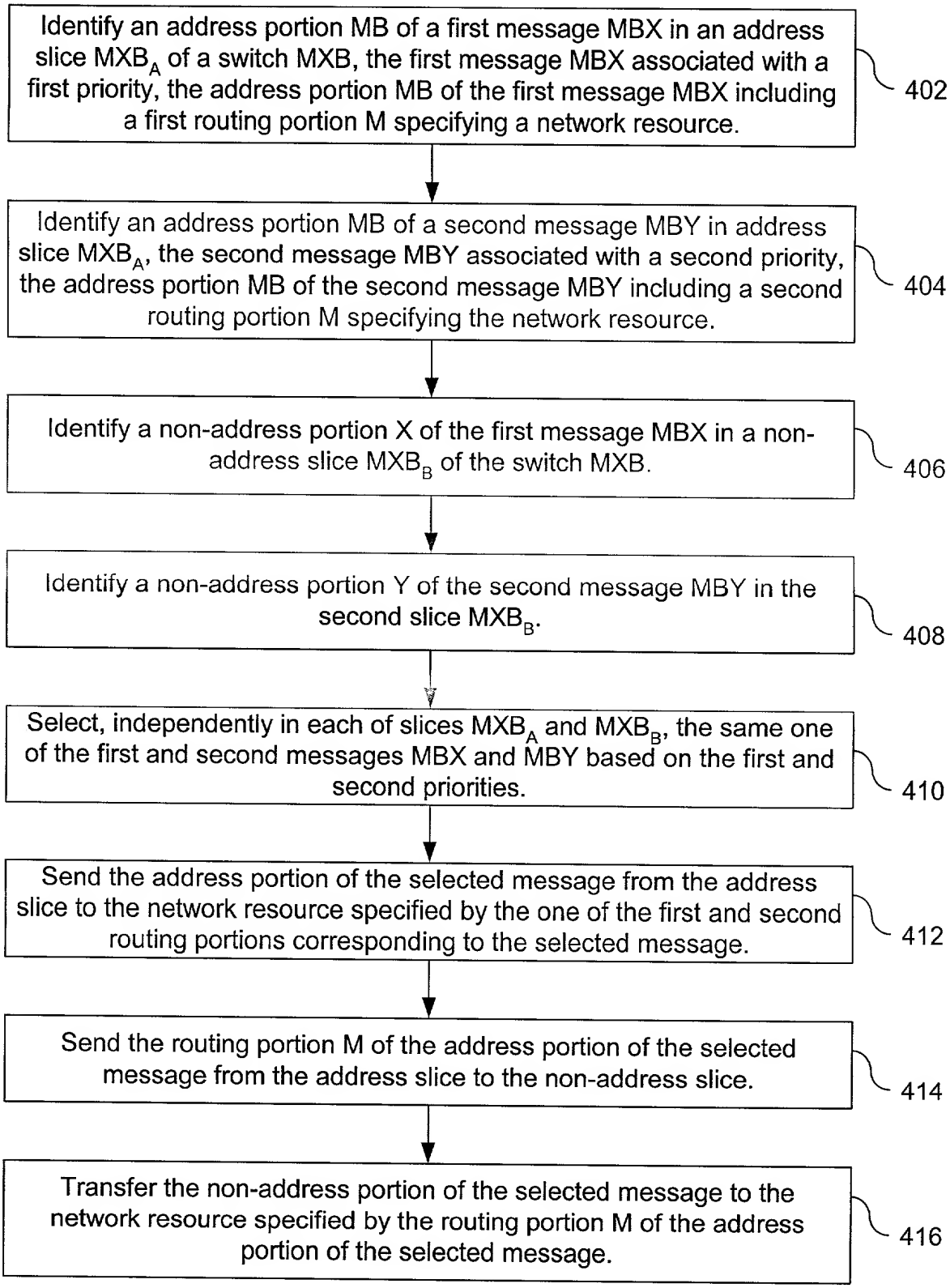

Identify an address portion MB of a first message MBX in an address slice MXB_A of a switch MXB, the first message MBX associated with a first priority, the address portion MB of the first message MBX including a first routing portion M specifying a network resource.
402
Identify an address portion MB of a second message MBY in address slice MXB_A, the second message MBY associated with a second priority, the address portion MB of the second message MBY including a second routing portion M specifying the network resource.
404
Identify a non-address portion X of the first message MBX in a non-address slice MXB_B of the switch MXB.
406
Identify a non-address portion Y of the second message MBY in the second slice MXB_B.
408
Select, independently in each of slices MXB_A and MXB_B, the same one of the first and second messages MBX and MBY based on the first and second priorities.
410
Send the address portion of the selected message from the address slice to the network resource specified by the one of the first and second routing portions corresponding to the selected message.
412
Send the routing portion M of the address portion of the selected message from the address slice to the non-address slice.
414
Transfer the non-address portion of the selected message to the network resource specified by the routing portion M of the address portion of the selected message.
416

FIG. 4

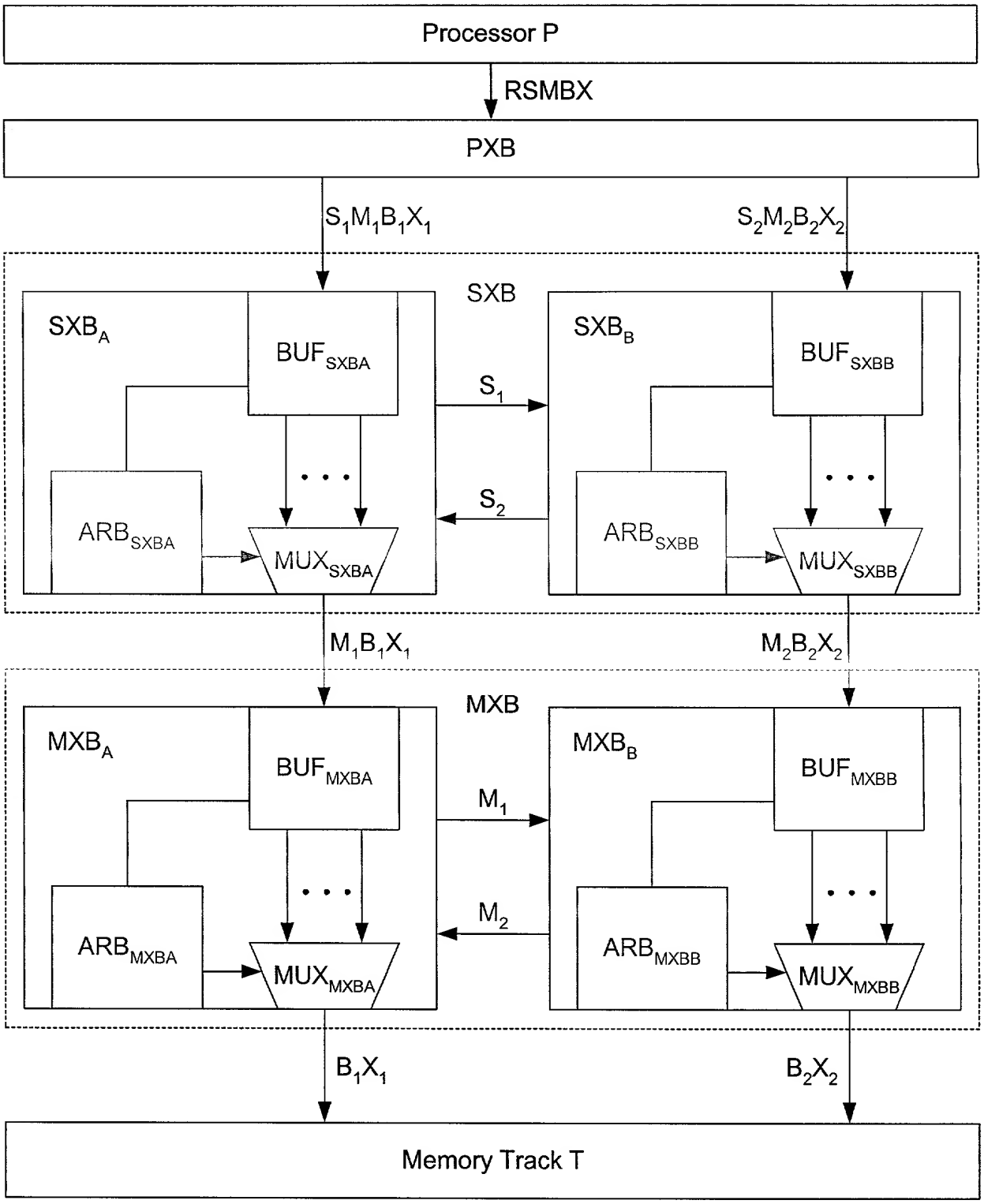

Processor P
RSMBX
PXB
$S_1M_1B_1X_1$
$S_2M_2B_2X_2$
SXB
SXB_A
BUF_{SXBA}
SXB_B
BUF_{SXBB}
S_1
S_2
ARB_{SXBA}
MUX_{SXBA}
ARB_{SXBB}
MUX_{SXBB}
$M_1B_1X_1$
$M_2B_2X_2$
MXB
MXB_A
BUF_{MXBA}
MXB_B
BUF_{MXBB}
M_1
M_2
ARB_{MXBA}
MUX_{MXBA}
ARB_{MXBB}
MUX_{MXBB}
B_1X_1
B_2X_2
Memory Track T

FIG. 5

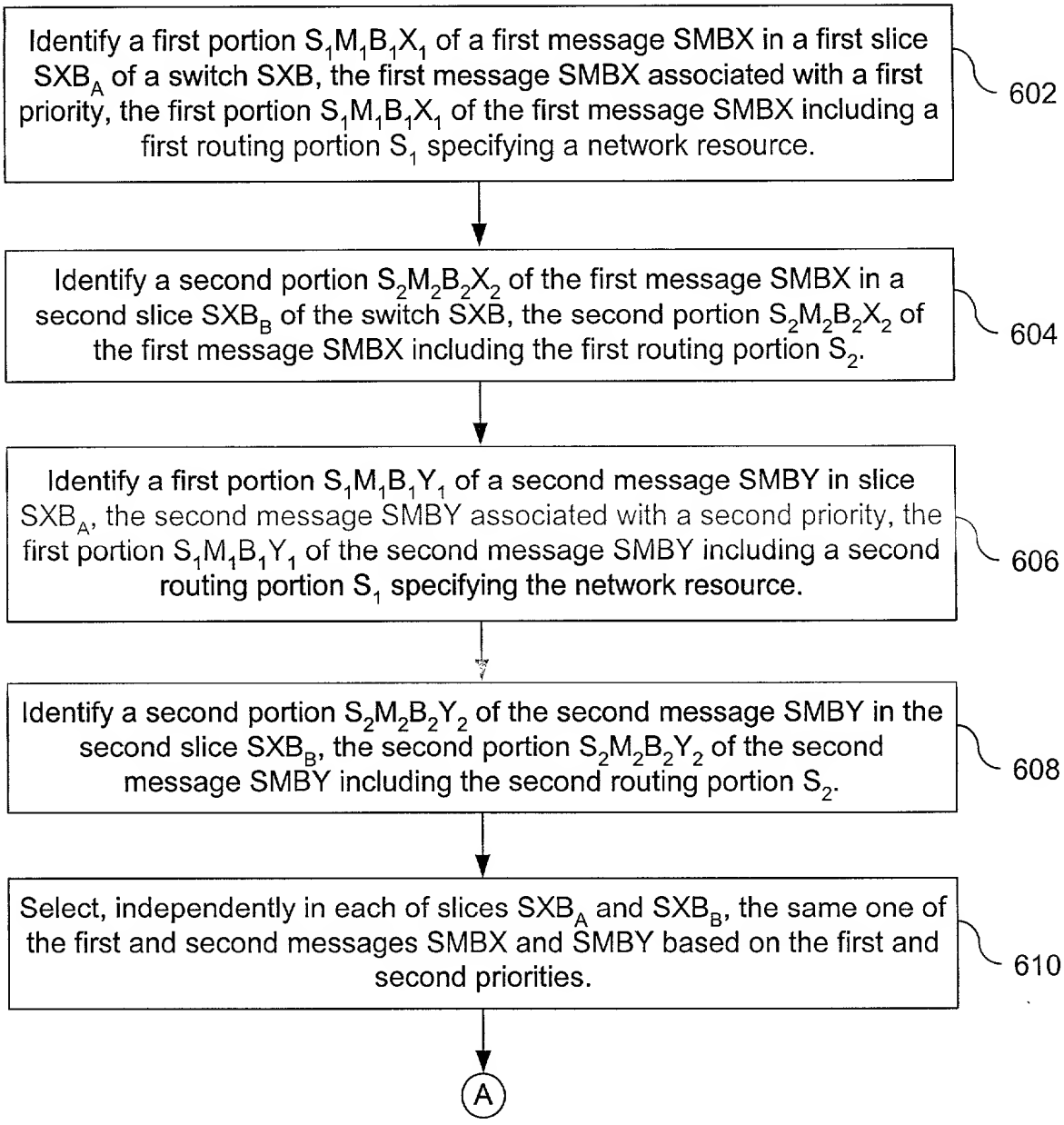

Identify a first portion $S_1M_1B_1X_1$ of a first message SMBX in a first slice SXB_A of a switch SXB, the first message SMBX associated with a first priority, the first portion $S_1M_1B_1X_1$ of the first message SMBX including a first routing portion S_1 specifying a network resource.
602
Identify a second portion $S_2M_2B_2X_2$ of the first message SMBX in a second slice SXB_B of the switch SXB, the second portion $S_2M_2B_2X_2$ of the first message SMBX including the first routing portion S_2.
604
Identify a first portion $S_1M_1B_1Y_1$ of a second message SMBY in slice SXB_A, the second message SMBY associated with a second priority, the first portion $S_1M_1B_1Y_1$ of the second message SMBY including a second routing portion S_1 specifying the network resource.
606
Identify a second portion $S_2M_2B_2Y_2$ of the second message SMBY in the second slice SXB_B, the second portion $S_2M_2B_2Y_2$ of the second message SMBY including the second routing portion S_2.
608
Select, independently in each of slices SXB_A and SXB_B, the same one of the first and second messages SMBX and SMBY based on the first and second priorities.
610
A

FIG. 6A

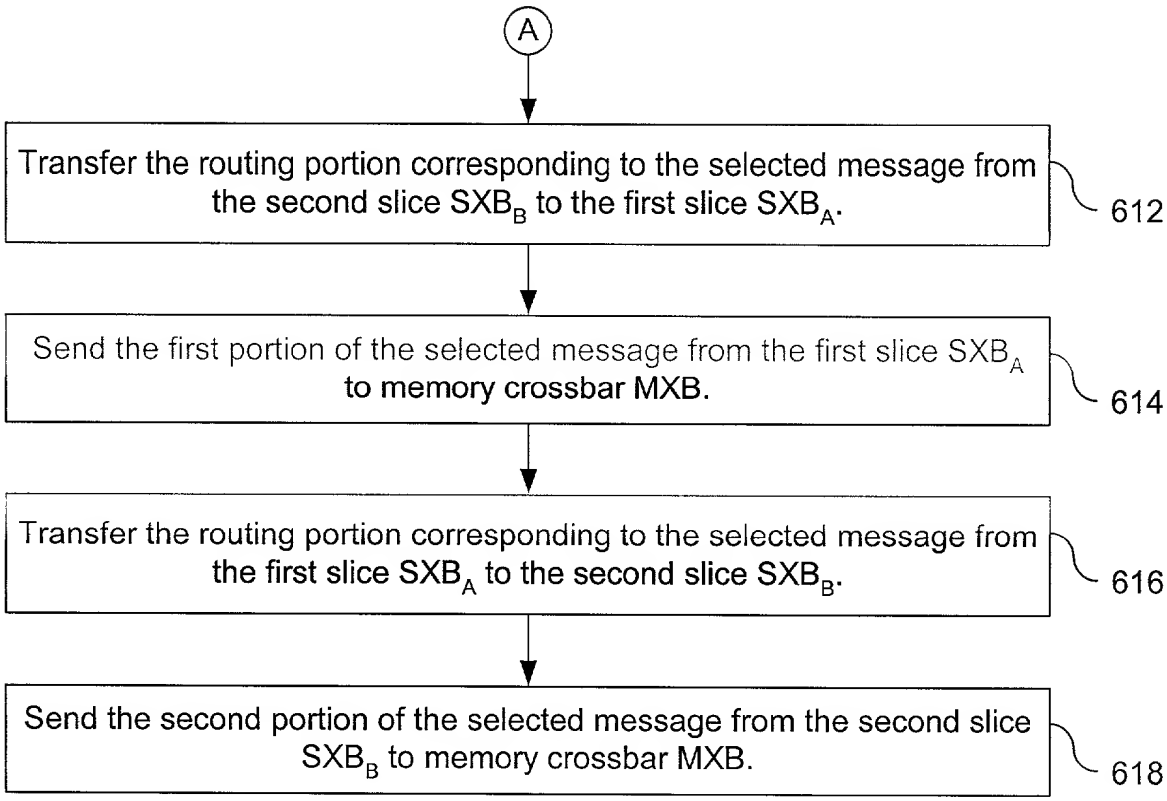

A
Transfer the routing portion corresponding to the selected message from the second slice SXB_B to the first slice SXB_A.
612
Send the first portion of the selected message from the first slice SXB_A to memory crossbar MXB.
614
Transfer the routing portion corresponding to the selected message from the first slice SXB_A to the second slice SXB_B.
616
Send the second portion of the selected message from the second slice SXB_B to memory crossbar MXB.
618

FIG. 6B

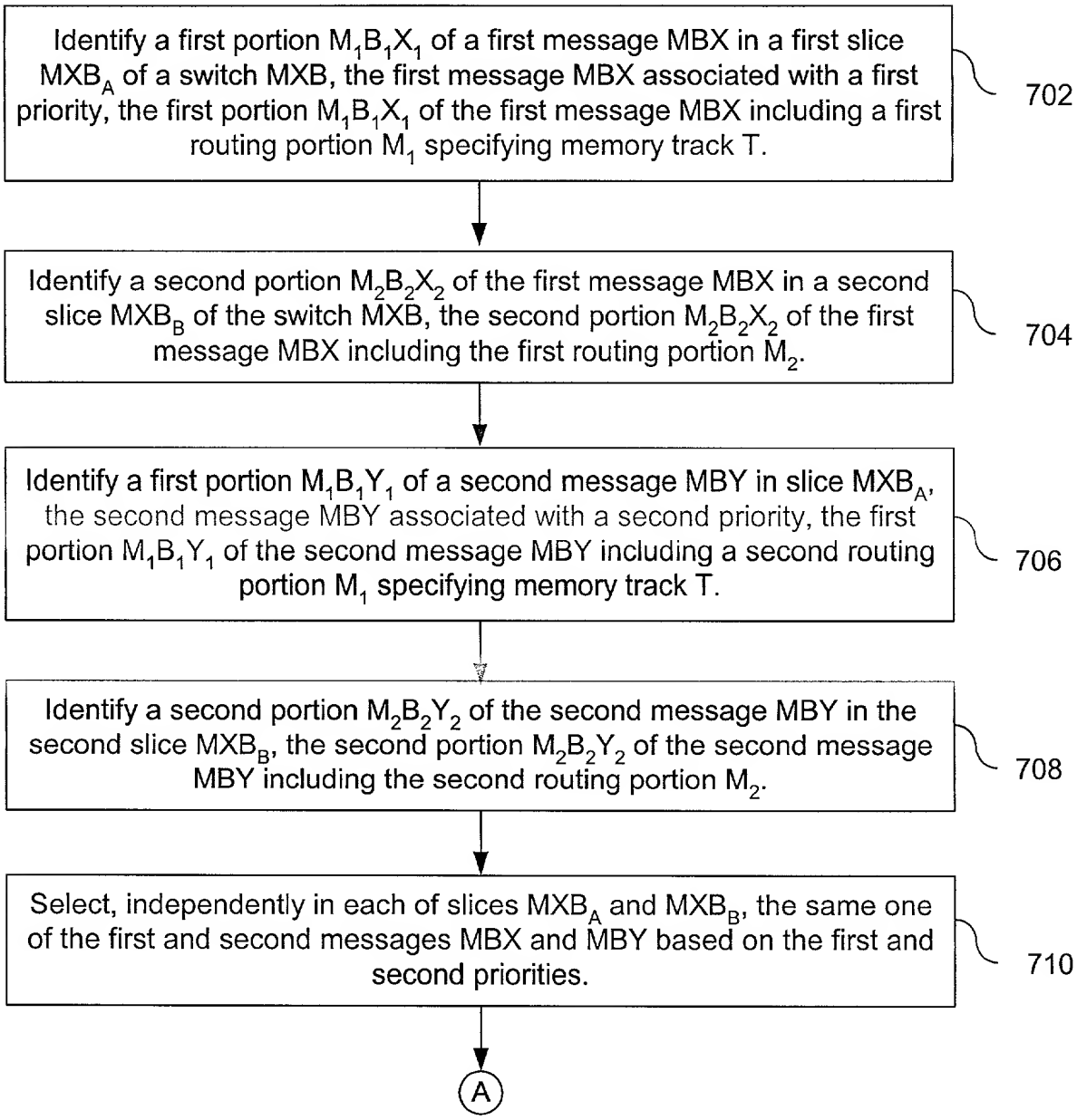

Identify a first portion $M_1B_1X_1$ of a first message MBX in a first slice MXB_A of a switch MXB, the first message MBX associated with a first priority, the first portion $M_1B_1X_1$ of the first message MBX including a first routing portion M_1 specifying memory track T.
702
Identify a second portion $M_2B_2X_2$ of the first message MBX in a second slice MXB_B of the switch MXB, the second portion $M_2B_2X_2$ of the first message MBX including the first routing portion M_2.
704
Identify a first portion $M_1B_1Y_1$ of a second message MBY in slice MXB_A, the second message MBY associated with a second priority, the first portion $M_1B_1Y_1$ of the second message MBY including a second routing portion M_1 specifying memory track T.
706
Identify a second portion $M_2B_2Y_2$ of the second message MBY in the second slice MXB_B, the second portion $M_2B_2Y_2$ of the second message MBY including the second routing portion M_2.
708
Select, independently in each of slices MXB_A and MXB_B, the same one of the first and second messages MBX and MBY based on the first and second priorities.
710
A

FIG. 7A

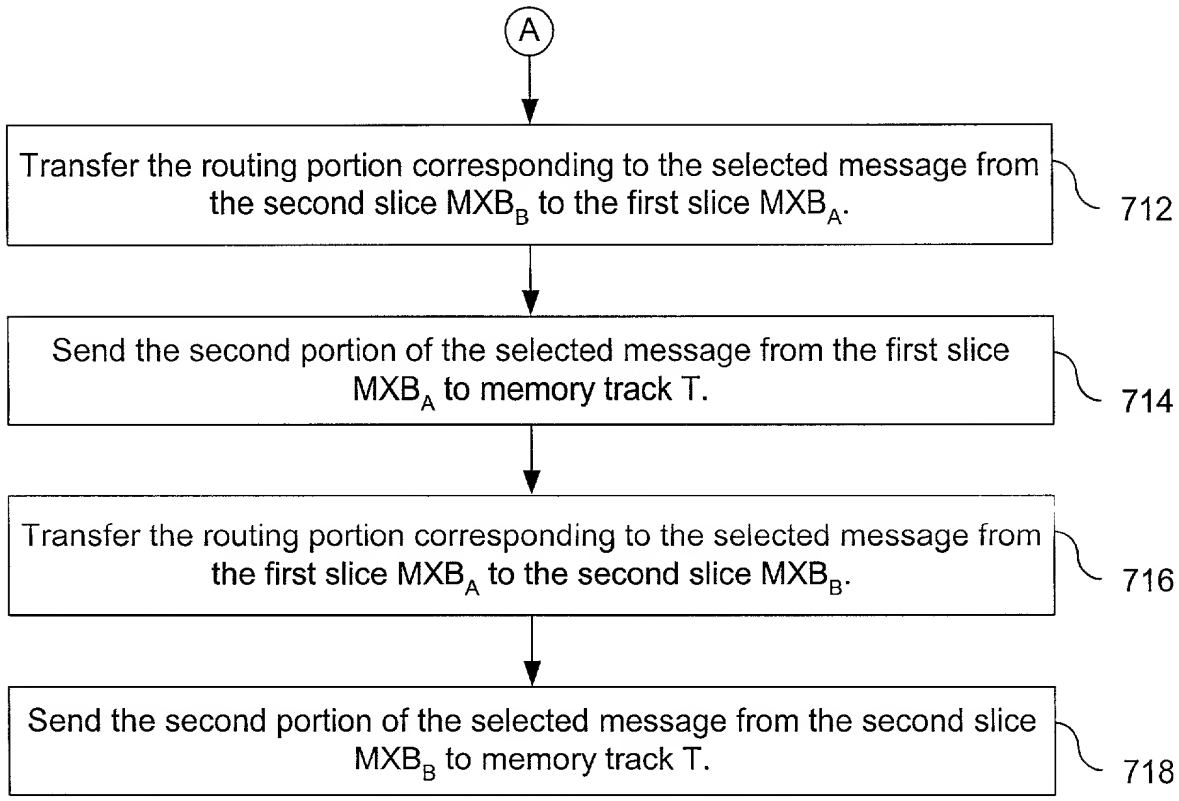

A
Transfer the routing portion corresponding to the selected message from the second slice MXB_B to the first slice MXB_A.
712
Send the second portion of the selected message from the first slice MXB_A to memory track T.
714
Transfer the routing portion corresponding to the selected message from the first slice MXB_A to the second slice MXB_B.
716
Send the second portion of the selected message from the second slice MXB_B to memory track T.
718

FIG. 7B

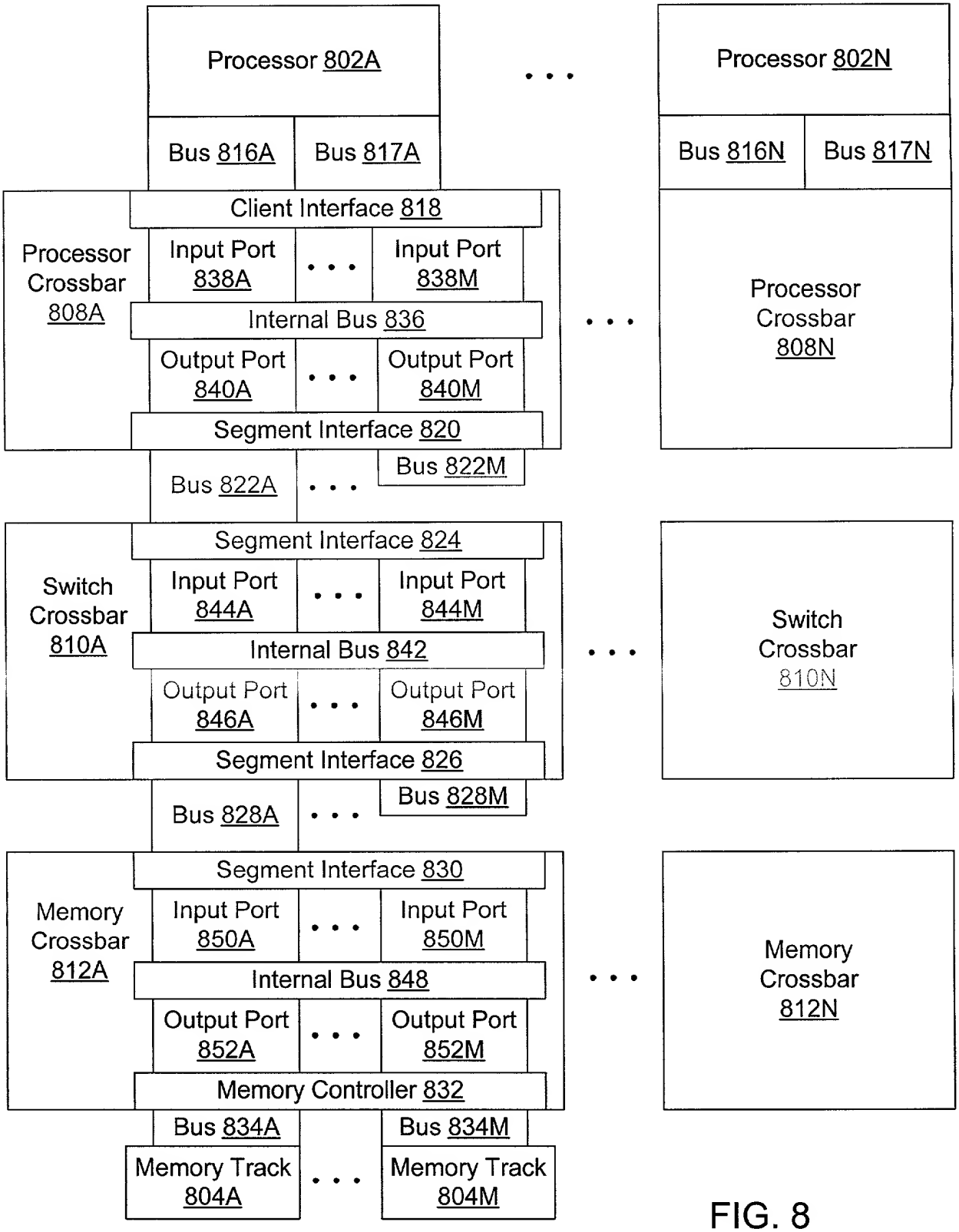
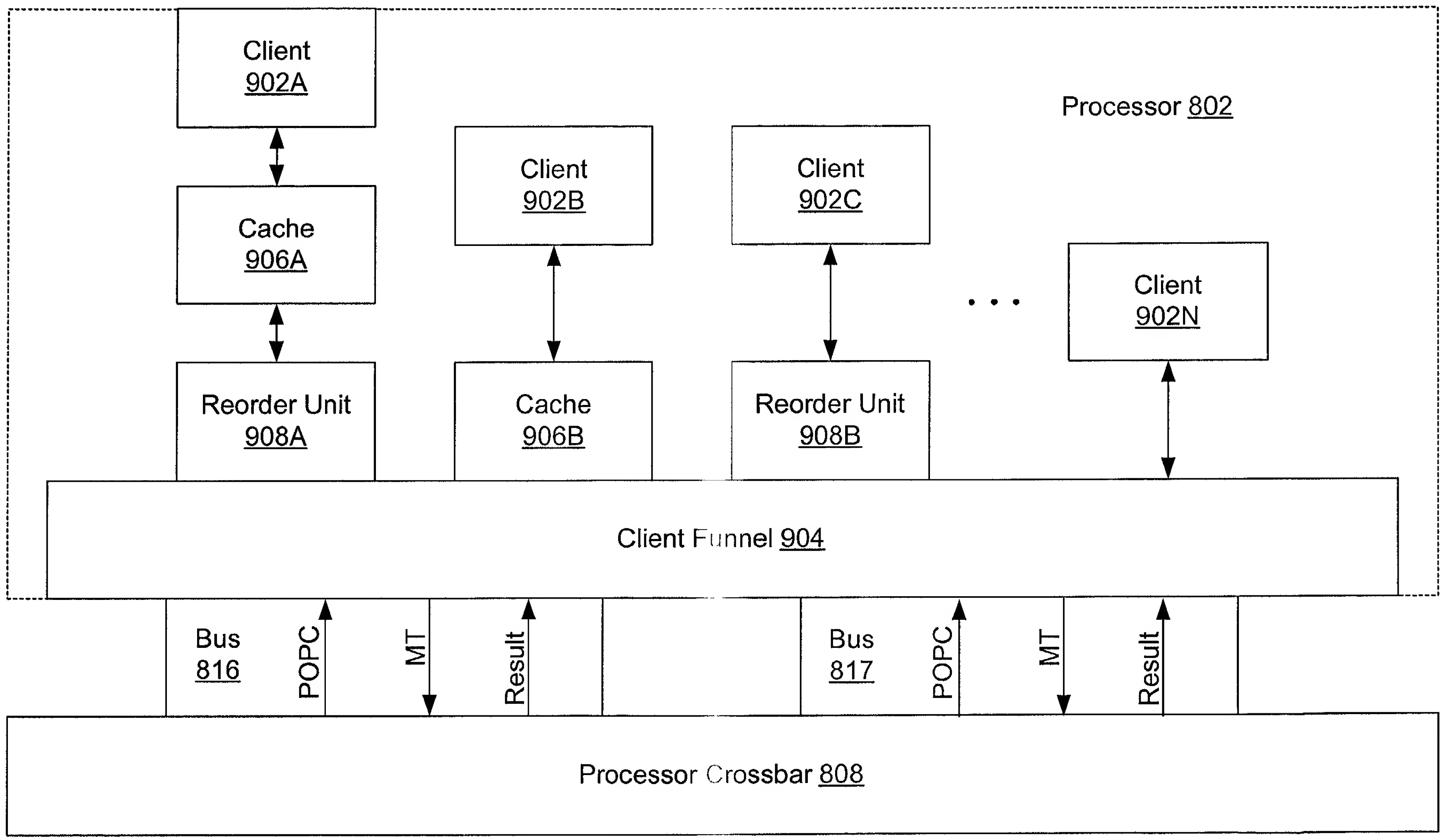

Processor 802A
Processor 802N
Bus 816A
Bus 817A
Bus 816N
Bus 817N
Client Interface 818
Processor Crossbar 808A
Input Port 838A
Input Port 838M
Internal Bus 836
Output Port 840A
Output Port 840M
Segment Interface 820
Bus 822A
Bus 822M
Processor Crossbar 808N
Segment Interface 824
Switch Crossbar 810A
Input Port 844A
Input Port 844M
Internal Bus 842
Output Port 846A
Output Port 846M
Segment Interface 826
Bus 828A
Bus 828M
Switch Crossbar 810N
Segment Interface 830
Memory Crossbar 812A
Input Port 850A
Input Port 850M
Internal Bus 848
Output Port 852A
Output Port 852M
Memory Controller 832
Bus 834A
Bus 834M
Memory Track 804A
Memory Track 804M
Memory Crossbar 812N

FIG. 8



Processor 802
Client 902A
Cache 906A
Reorder Unit 908A
Client 902B
Cache 906B
Client 902C
Reorder Unit 908B
Client 902N
Client Funnel 904
Bus 816
POPC
MT
Result
Bus 817
POPC
MT
Result
Processor Crossbar 808

FIG. 9

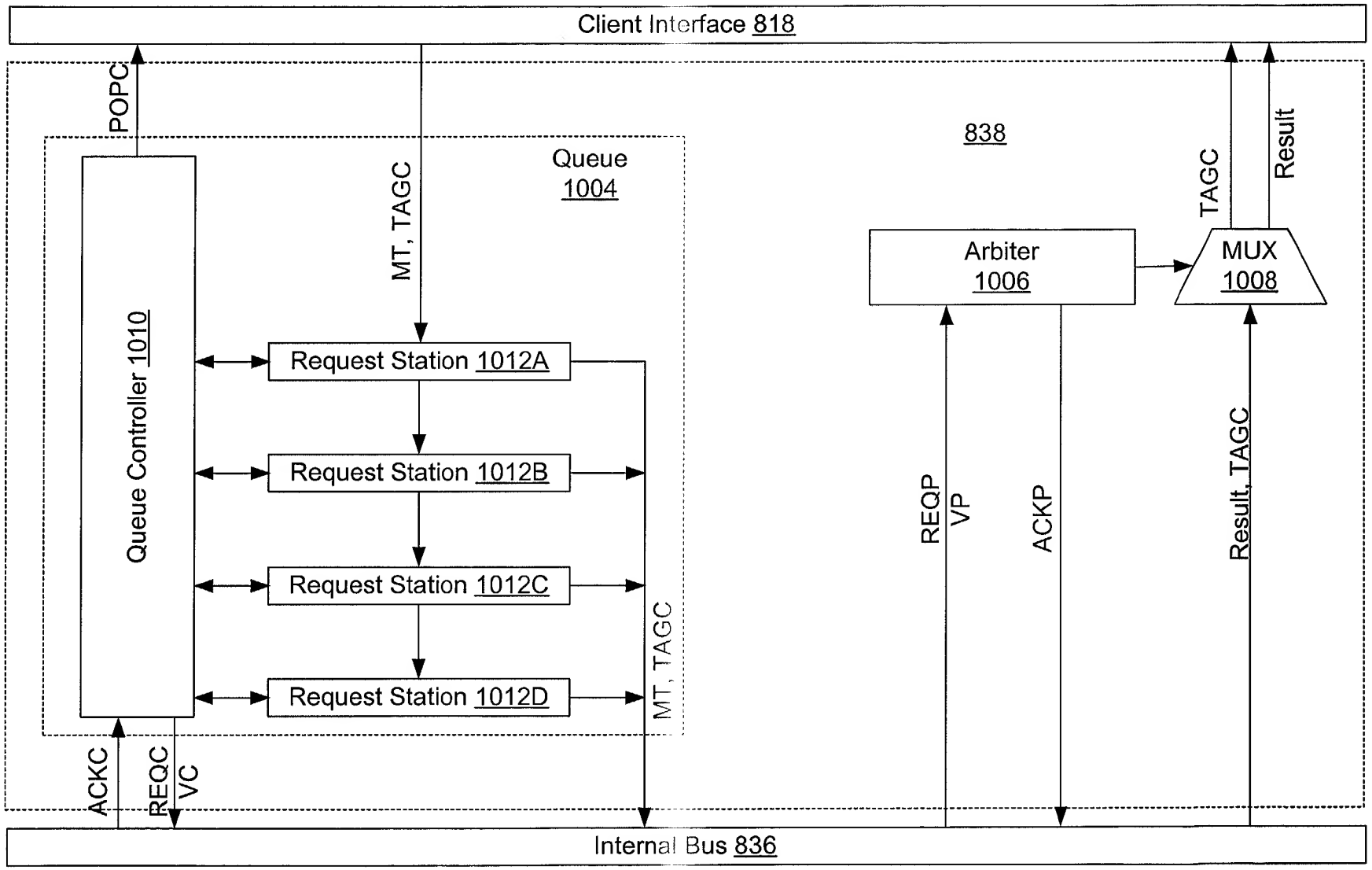

Client Interface 818
POPC
MT, TAGC
Queue
1004
838
TAGC
Result
Arbiter
1006
MUX
1008
Queue Controller 1010
Request Station 1012A
Request Station 1012B
Request Station 1012C
Request Station 1012D
REQP
VP
ACKP
Result, TAGC
MT, TAGC
ACKC
REQC
VC
Internal Bus 836

FIG. 10

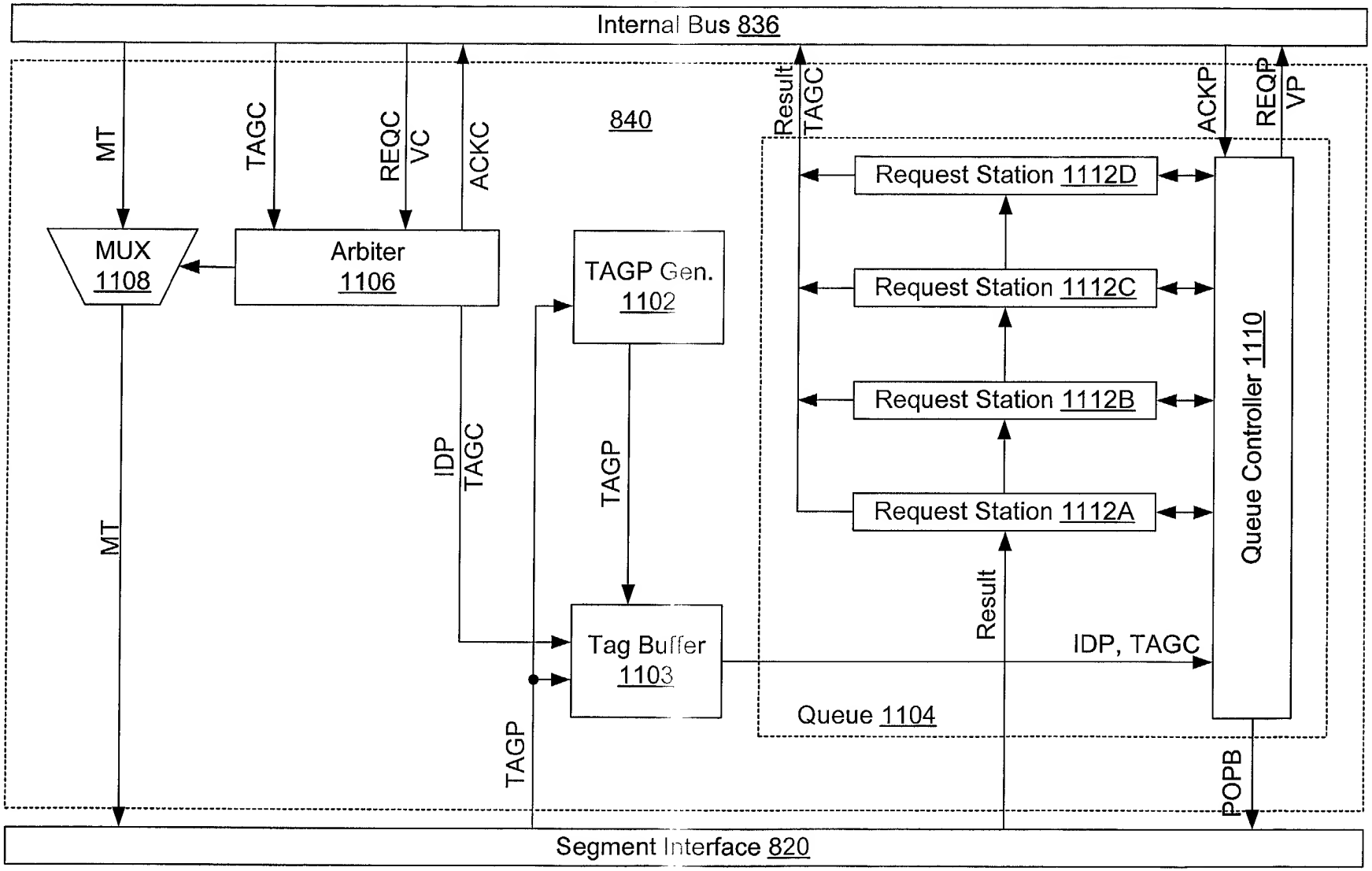

Internal Bus 836
840
MT
TAGC
REQC
VC
ACKC
Result
TAGC
ACKP
REQP
VP
MUX 1108
Arbiter 1106
TAGP Gen. 1102
Request Station 1112D
Request Station 1112C
Request Station 1112B
Request Station 1112A
Queue Controller 1110
IDP
TAGC
TAGP
MT
Result
IDP, TAGC
Tag Buffer 1103
Queue 1104
TAGP
POPB
Segment Interface 820

FIG. 11

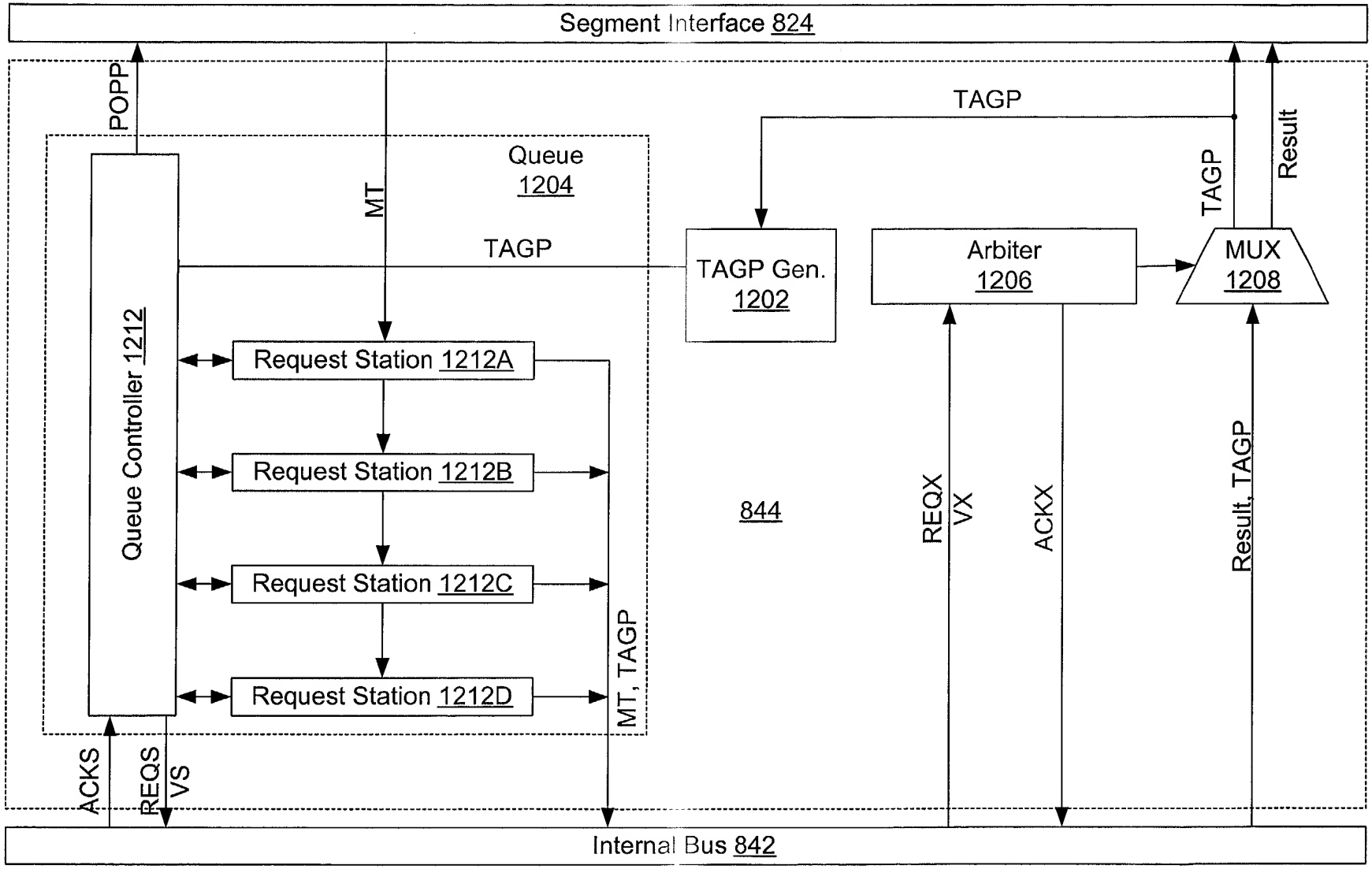

Segment Interface 824
POPP
Queue
1204
MT
TAGP
TAGP
Result
TAGP Gen.
1202
Arbiter
1206
MUX
1208
Queue Controller 1212
Request Station 1212A
Request Station 1212B
Request Station 1212C
Request Station 1212D
844
REQX
VX
ACKX
Result, TAGP
MT, TAGP
ACKS
REQS
VS
Internal Bus 842

FIG. 12

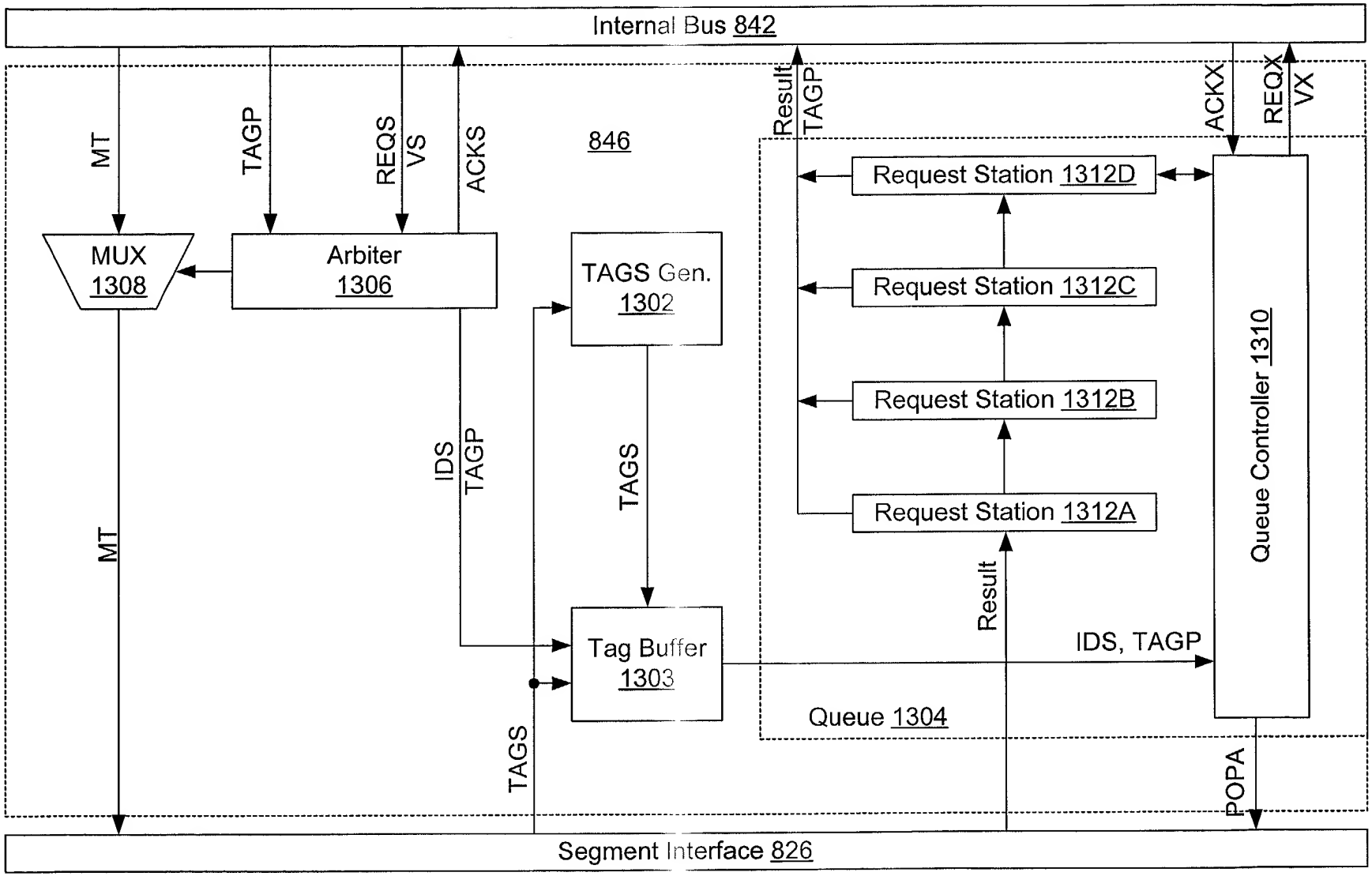

Internal Bus 842
MT
TAGP
REQS
VS
ACKS
846
Result
TAGP
ACKX
REQX
VX
MUX 1308
Arbiter 1306
TAGS Gen. 1302
Request Station 1312D
Request Station 1312C
Request Station 1312B
Request Station 1312A
Queue Controller 1310
IDS
TAGP
TAGS
MT
Result
IDS, TAGP
Tag Buffer 1303
Queue 1304
TAGS
POPA
Segment Interface 826

FIG. 13

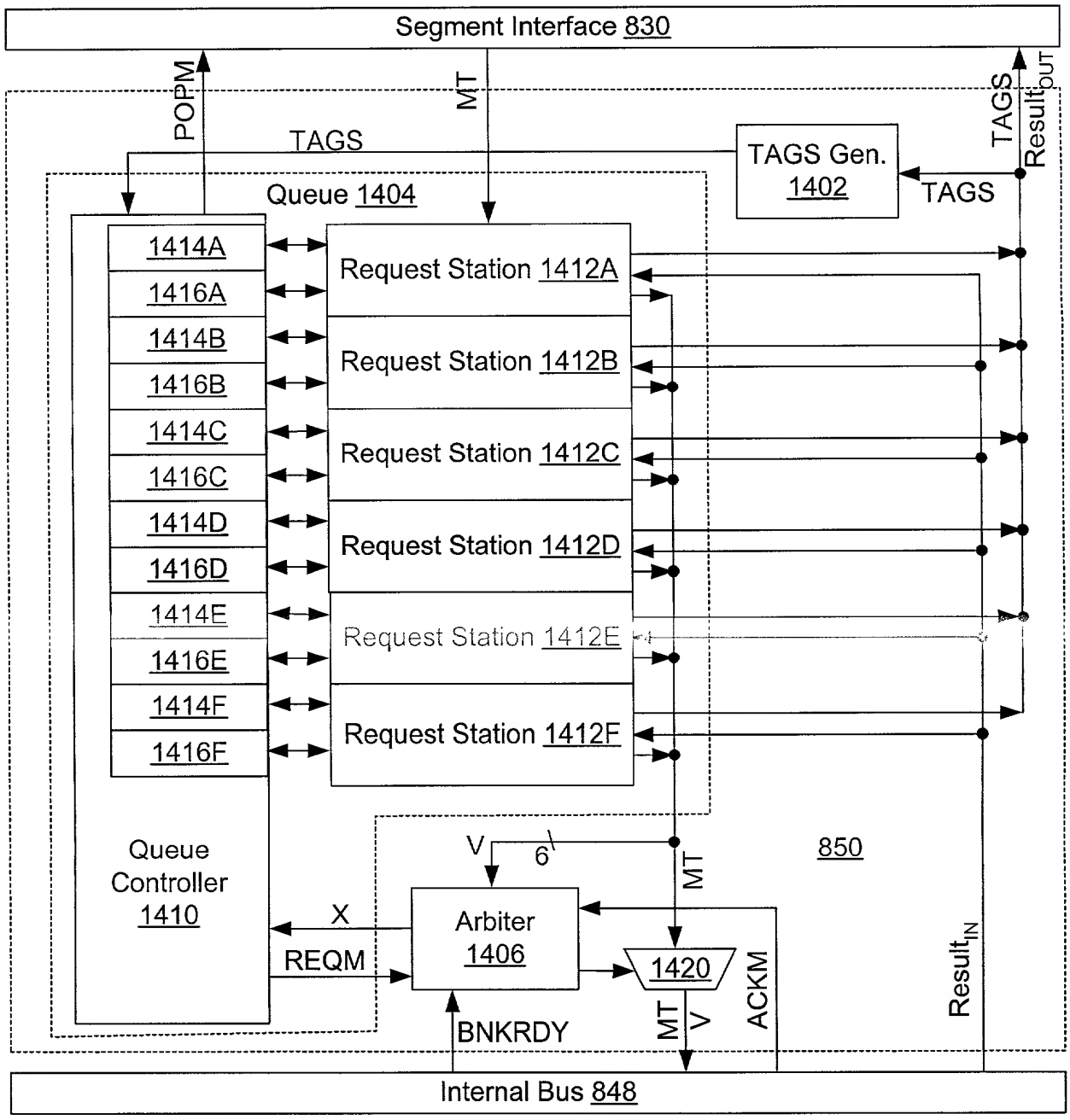

Segment Interface 830
POPM
MT
TAGS
TAGS Gen. 1402
TAGS
Result OUT
Queue 1404
1414A
1416A
1414B
1416B
1414C
1416C
1414D
1416D
1414E
1416E
1414F
1416F
Request Station 1412A
Request Station 1412B
Request Station 1412C
Request Station 1412D
Request Station 1412E
Request Station 1412F
Queue Controller 1410
V
6
MT
850
X
REQM
Arbiter 1406
1420
ACKM
BNKRDY
MT
V
Result IN
Internal Bus 848

FIG. 14

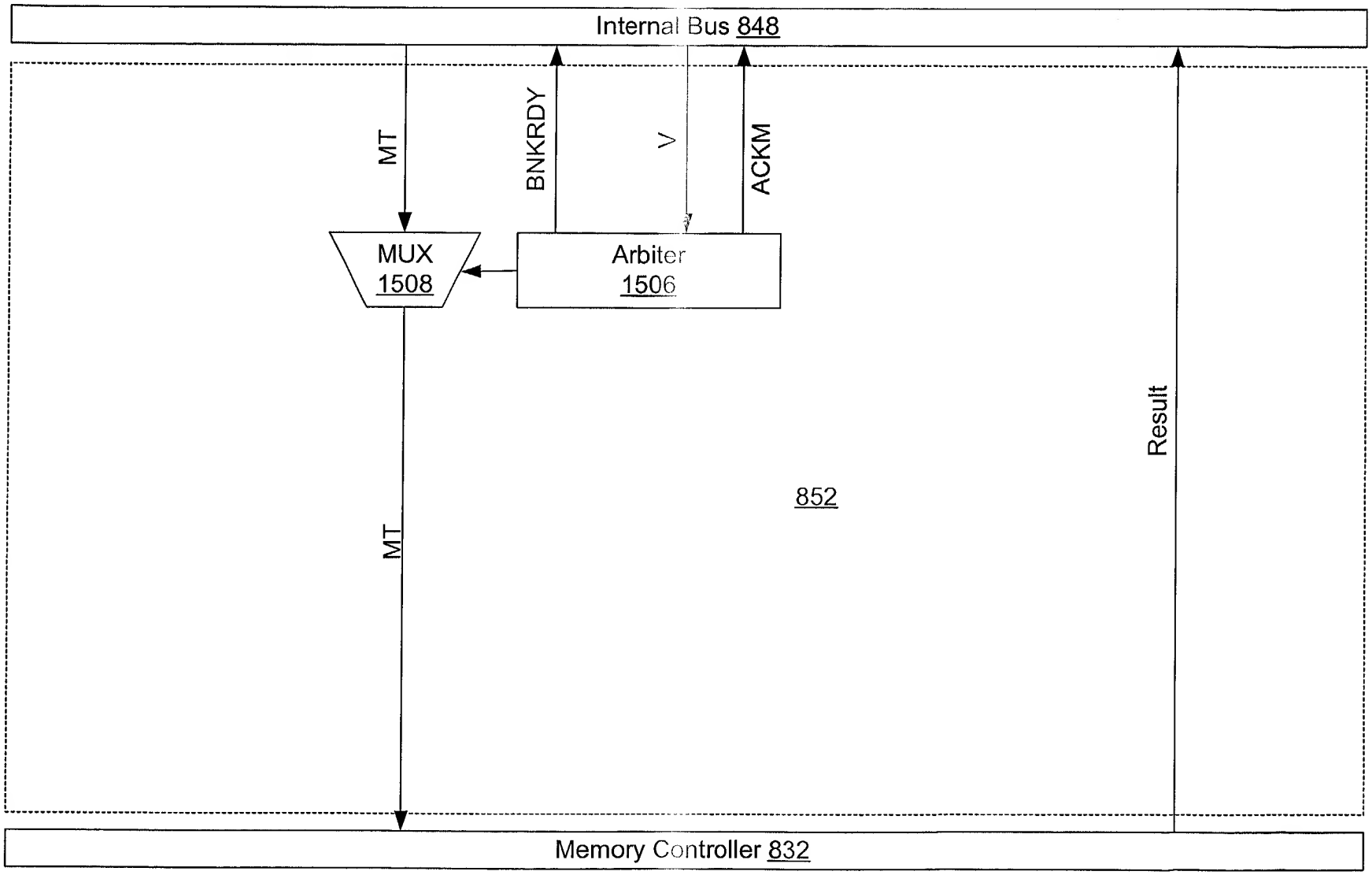

Internal Bus 848
MT
BNKRDY
V
ACKM
MUX
1508
Arbiter
1506
Result
852
MT
Memory Controller 832

FIG. 15

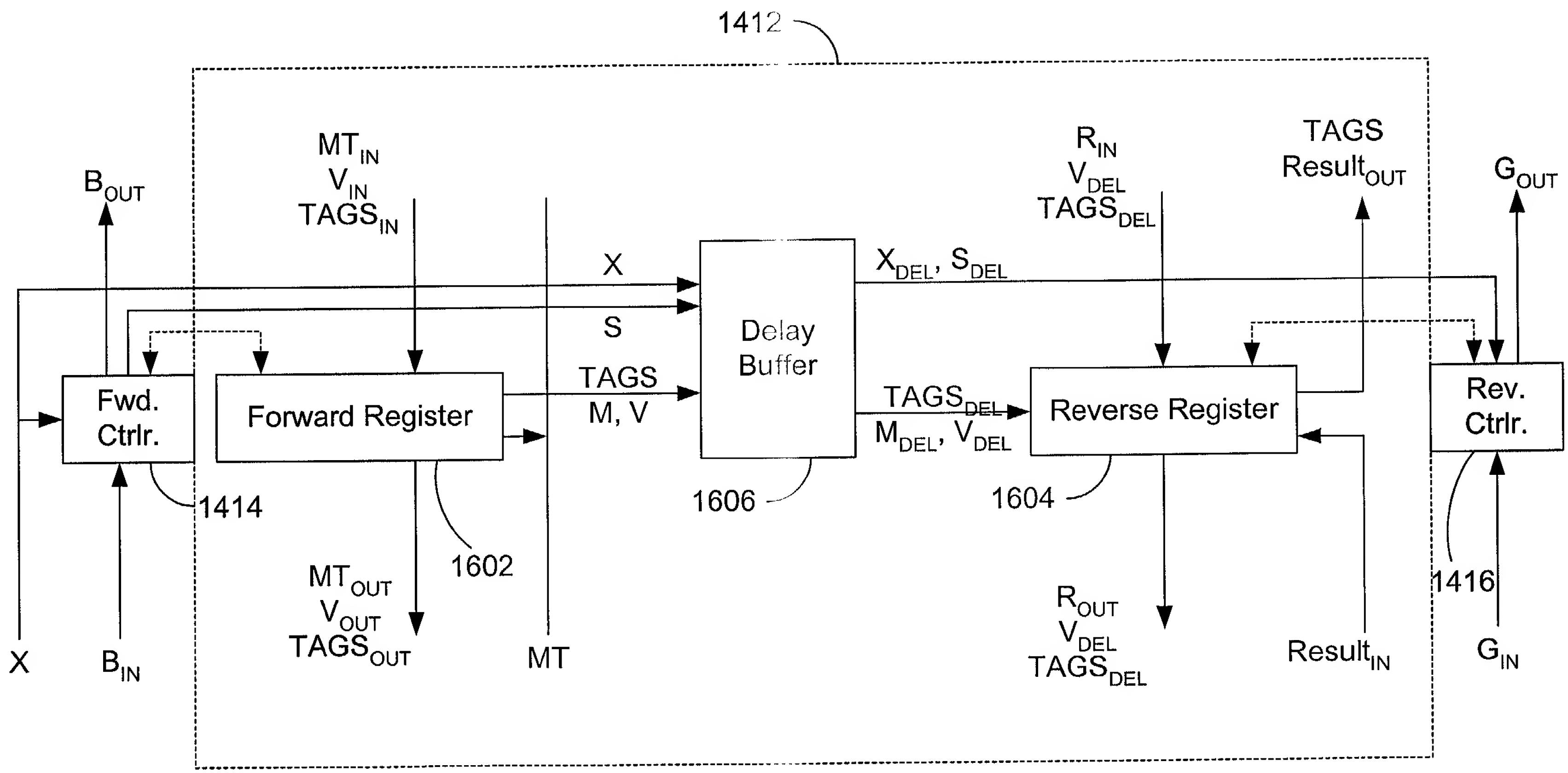

1412
MT_{IN}
V_{IN}
$TAGS_{IN}$
B_{OUT}
X
S
TAGS
M, V
Delay
Buffer
X_{DEL}, S_{DEL}
R_{IN}
V_{DEL}
$TAGS_{DEL}$
TAGS
$Result_{OUT}$
G_{OUT}
Fwd.
Ctrlr.
Forward Register
$TAGS_{DEL}$
M_{DEL}, V_{DEL}
Reverse Register
Rev.
Ctrlr.
1414
1606
1604
1602
MT_{OUT}
V_{OUT}
$TAGS_{OUT}$
1416
R_{OUT}
V_{DEL}
$TAGS_{DEL}$
X
B_{IN}
MT
$Result_{IN}$
G_{IN}

FIG. 16

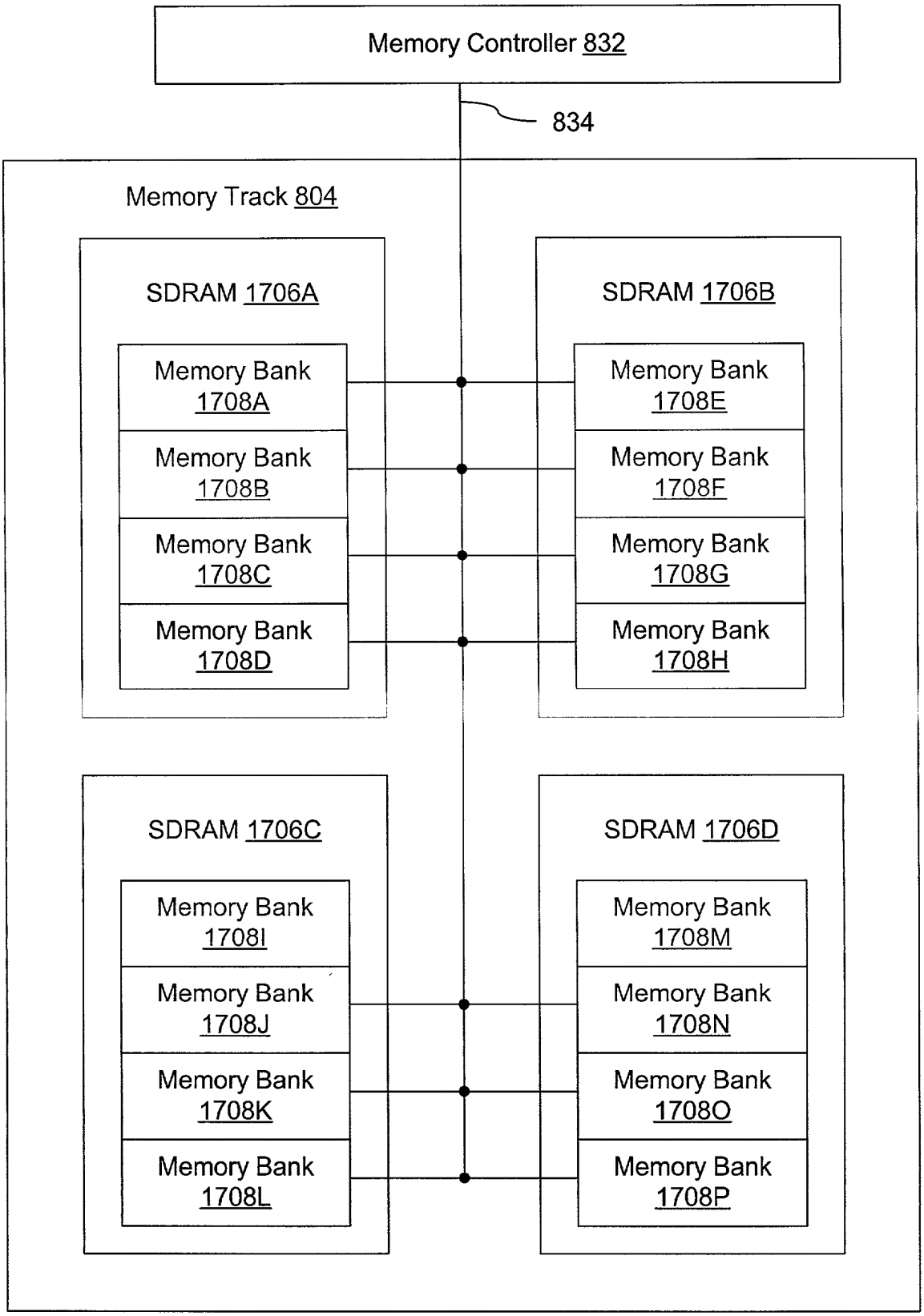

Memory Controller 832
834
Memory Track 804
SDRAM 1706A
Memory Bank 1708A
Memory Bank 1708B
Memory Bank 1708C
Memory Bank 1708D
SDRAM 1706B
Memory Bank 1708E
Memory Bank 1708F
Memory Bank 1708G
Memory Bank 1708H
SDRAM 1706C
Memory Bank 1708I
Memory Bank 1708J
Memory Bank 1708K
Memory Bank 1708L
SDRAM 1706D
Memory Bank 1708M
Memory Bank 1708N
Memory Bank 1708O
Memory Bank 1708P

FIG. 17

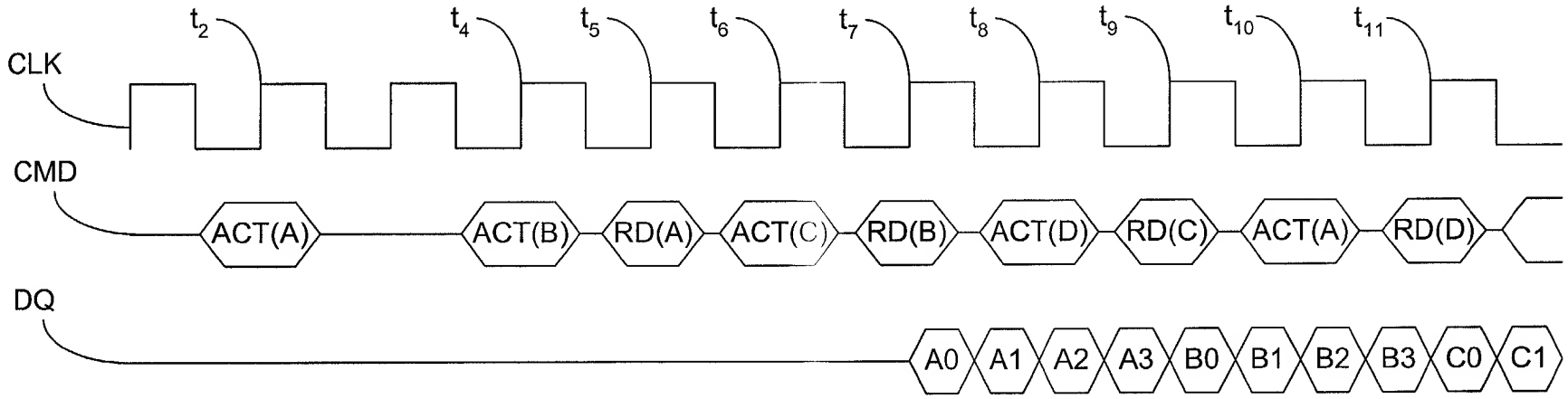

t2
t4
t5
t6
t7
t8
t9
t10
t11
CLK
CMD
ACT(A)
ACT(B)
RD(A)
ACT(C)
RD(B)
ACT(D)
RD(C)
ACT(A)
RD(D)
DQ
A0
A1
A2
A3
B0
B1
B2
B3
C0
C1

FIG. 18

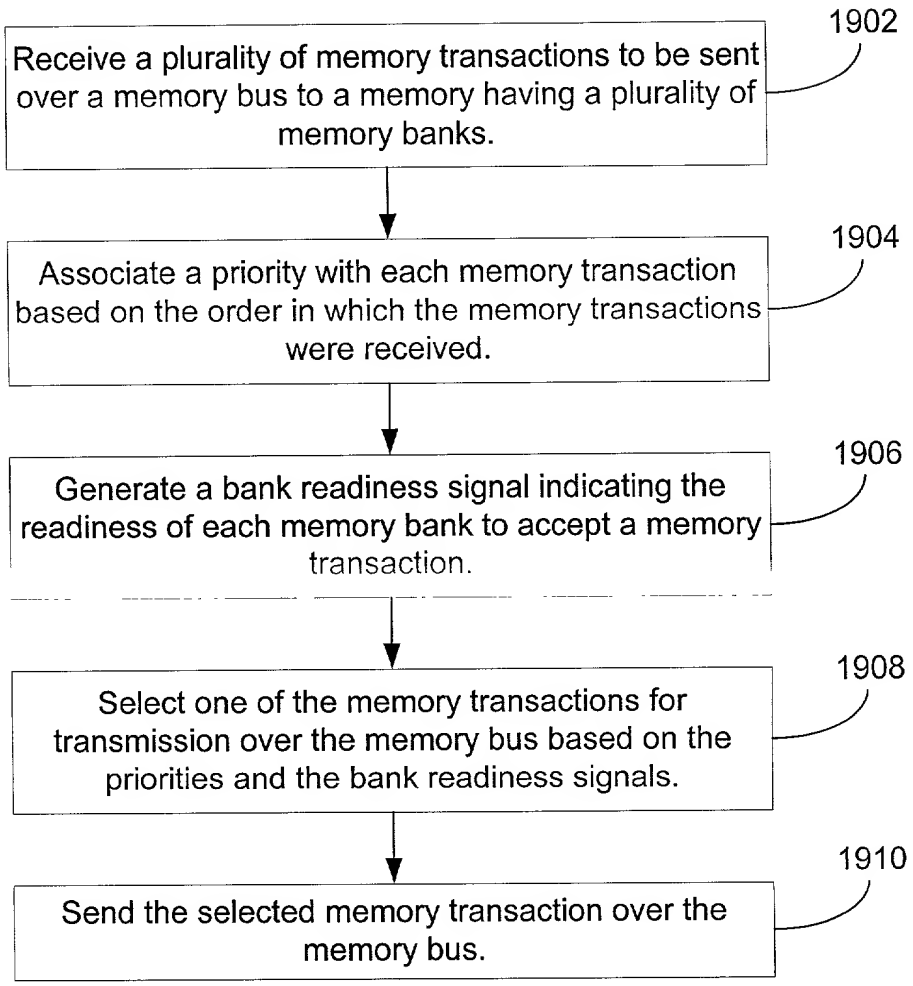

Receive a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks.
1902
Associate a priority with each memory transaction based on the order in which the memory transactions were received.
1904
Generate a bank readiness signal indicating the readiness of each memory bank to accept a memory transaction.
1906
Select one of the memory transactions for transmission over the memory bus based on the priorities and the bank readiness signals.
1908
Send the selected memory transaction over the memory bus.
1910

FIG. 19

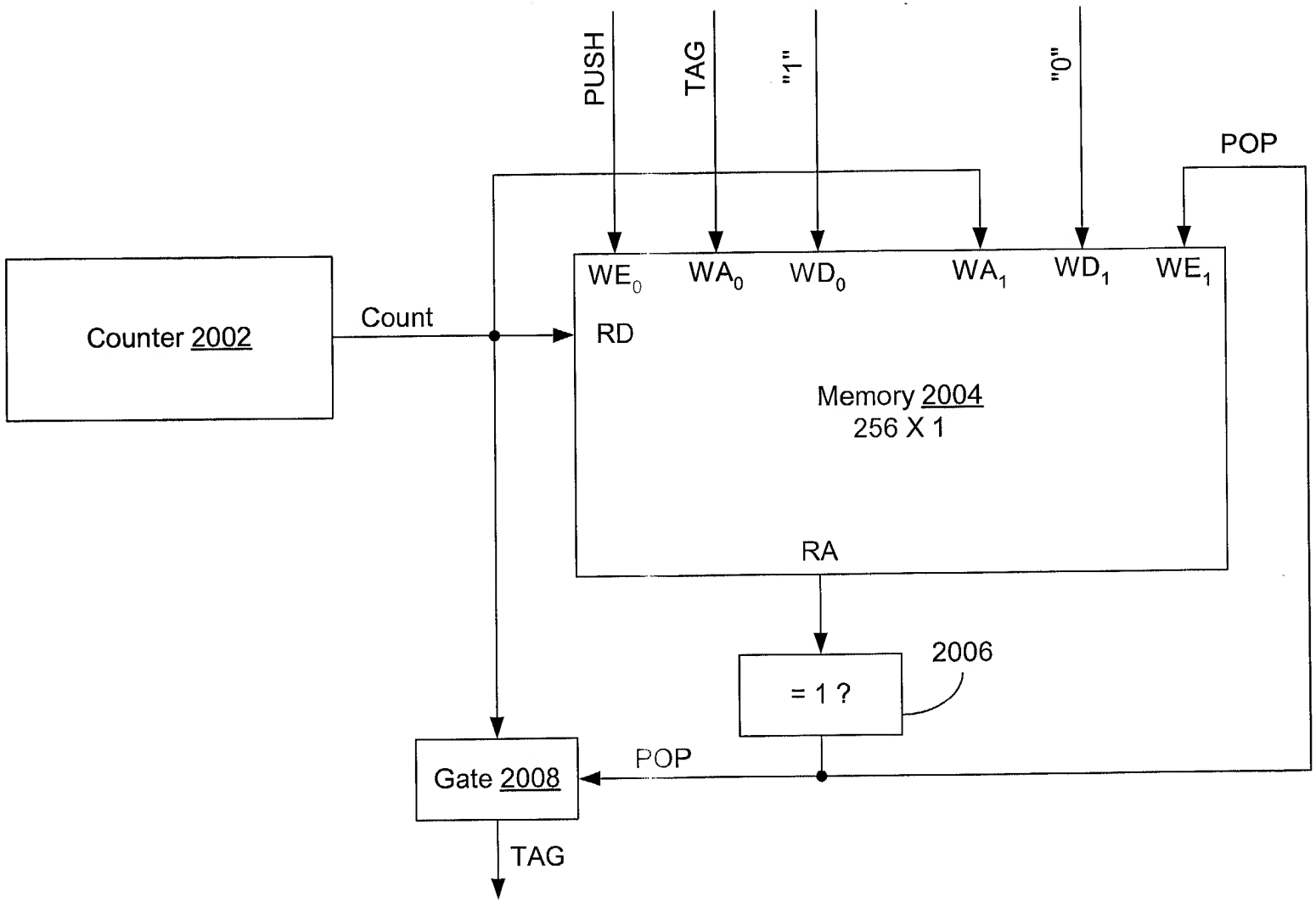

PUSH
TAG
"1"
"0"
POP
WE0
WA0
WD0
WA1
WD1
WE1
Counter 2002
Count
RD
Memory 2004
256 X 1
RA
2006
= 1 ?
Gate 2008
POP
TAG

FIG. 20

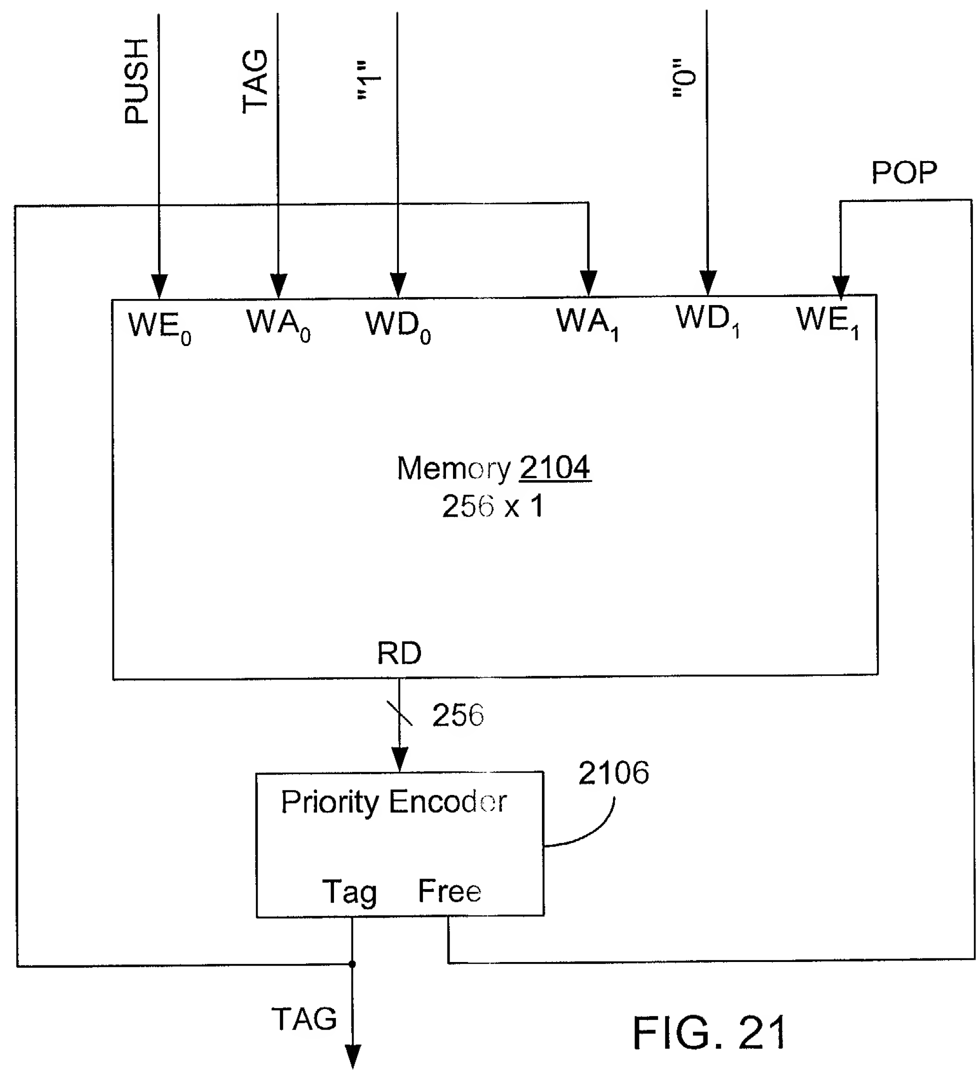

PUSH
TAG
"1"
"0"
POP
WE0
WA0
WD0
WA1
WD1
WE1
Memory 2104
256 x 1
RD
256
Priority Encoder
2106
Tag
Free
TAG

FIG. 21